What is claimed is:

1. A method of patterning metal layers of a semiconductor wafer, the method comprising:

depositing a first conductive layer over a substrate;

depositing an insulating layer over the first conductive layer;

depositing a second conductive layer over the insulating layer;

depositing a first resist over the second conductive layer;

depositing a second resist over the first resist;

patterning the first resist with a first pattern and patterning the second resist with a second pattern; and

simultaneously transferring the first pattern to the first conductive layer and the second pattern to the second conductive layer.

2. The method according to Claim 1 wherein transferring the first and second patterns comprise exposing the wafer to a single reactive ion etch process.

3. The method according to Claim 1 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

4. The method according to Claim 1 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

5. The method according to Claim 1 wherein the insulating layer comprises a capacitor dielectric, wherein transferring the first pattern to the first conductive layer comprises forming bottom metal plates of a MIM capacitor, and wherein transferring the second pattern to the second conductive layer comprises forming top metal plates of the MIM capacitor.

6. The method according to Claim 1 further comprising transferring the first pattern to the insulating layer.

7. A method of patterning metal layers of a semiconductor wafer, the wafer comprising a first conductive layer, an insulating layer disposed over the first conductive layer and a second conductive layer disposed over the insulating layer, the method comprising:

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist;

patterning the second resist with a second pattern;

simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer.

8. The method according to Claim 7 wherein transferring the first and second patterns comprise exposing the wafer to a reactive ion etch process.

9. The method according to Claim 8 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

10. The method according to Claim 8 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

11. The method according to Claim 8 wherein the insulating layer comprises a capacitor dielectric, wherein transferring the first pattern to the first conductive layer comprises forming bottom metal plates of a MIM capacitor, and wherein transferring the second pattern to the second conductive layer comprises forming top metal plates of the MIM capacitor.

12. The method according to Claim 7 further comprising transferring the first pattern to the insulating layer.

13. A method of forming capacitive plates of a MIM capacitor, comprising:

providing a wafer having a substrate;

depositing a first conductive layer on the substrate;

depositing a capacitor dielectric layer over the first conductive layer;

depositing a second conductive layer over the capacitor dielectric layer;

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist;

patterning the second resist with a second pattern;

simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer.

14. The method according to Claim 13 wherein transferring the first and second patterns comprise exposing the wafer to a reactive ion etch process.

15. The method according to Claim 13 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

16. The method according to Claim 13 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

17. The method according to Claim 13 further comprising transferring the first pattern to the insulating layer.